In the Claims

This listing of claims will replace all prior listings, and versions, of claims in the application.

1-3. (Canceled)

4. (Currently Amended) An array panel comprising:

a substrate;

a gate line extended on the substrate in a first direction;

a data line extended on the substrate in a second direction;

a switching element including a gate electrode, a source electrode, and a drain electrode, the switching element being formed in a pixel region ~~defined by the gate and the data lines~~;

a photoelectric cell for generating electrons in proportion with the intensity of light supplied from outside, thereby generating an electrical signal;

a pixel electrode formed in the pixel region, the pixel electrode gathering electrons generated from the photoelectric cell;

a storage capacitor formed in the pixel region, the storage capacitor storing the electrons gathered by the pixel electrode, wherein the storage capacitor comprises a capacitor electrode, a first transparent electrode formed directly on the capacitor electrode, an insulating layer, and the pixel electrode formed directly on the insulating layer;

a gate driver making an electrical contact with an end portion of the gate line on the substrate, the gate driver sequentially providing a scan signal for driving the switching element; and

a data pad making an electrical contact with an end portion of the data line on the substrate, the electrons stored in the storage capacitor being extracted to the data pad through the switching element in case that the switching element is turned on.

5. (Original) The array panel of claim 4, wherein the gate driver includes a plurality of stages sequentially making an electrical contact with each other, each stage including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage

being sequentially outputted from each output terminal, so that the stages function as a shift register.

6. (Original) The array panel of claim 4, further comprising an organic layer interposed between the pixel electrode and the switching element.

7. (Original) The array panel of claim 4, further comprising an organic layer interposed between the pixel electrode and the gate driver.

8. (Original) The array panel of claim 4, wherein the pixel electrode comprises indium tin oxide (ITO).

9. (Original) The array panel of claim 4, wherein the pixel electrode is disposed on a whole surface of the switching element.

10. (Original) The array panel of claim 4, wherein the pixel electrode is disposed on a whole surface of the gate driver.

11. (Currently Amended) A method of manufacturing an array panel, the method comprising:

forming first and second switching elements, a first conductive line for a data pad and a second conductive line for a storage capacitor, the first switching element corresponding to a pixel region of a substrate;

forming a first transparent electrode on the first and second conductive lines; sequentially coating an insulating layer and an organic layer on the first transparent electrode;

partially removing the organic layer corresponding to the first and second conductive lines and a drain electrode of the first switching element by an exposure and development process;

partially removing the insulating layer ~~corresponding to the first and second conductive lines, thereby exposing~~ to form a contact hole extending to the first transparent electrode on the data pad and a drain contact hole extending to the drain electrode of the first switching element;

and

forming a second transparent electrode for collecting electrons, the second transparent electrode being directly ~~electrically~~ connected to the drain electrode and the first transparent electrode on the data pad ~~and the drain electrode~~, wherein the second transparent electrode over the second conductive line is formed on the insulating layer, thereby forming the storage capacitor between the second transparent electrode and the second conductive line.

12. (Currently Amended) The method of claim 11, further comprising: forming a protecting layer on the exposed organic layer and the second transparent electrode [[layer]];

forming a light conductive semiconductor layer on the protecting layer; and

forming an electrode on the light conductive semiconductor layer.

13. (Original) The method of claim 11, wherein the second transparent electrode is disposed on a whole surface of the first switching element.

14. (Original) The method of claim 11, wherein the second transparent electrode is disposed on a whole surface of the second switching element.

15. (Currently Amended) The method of claim 11, wherein the second switching element is a plurality of thin film transistors comprising amorphous silicon, said plurality of thin film transistors arranged in a plurality of stages sequentially making an electrical contact with each other, and each stage ~~transparent electrode includes a plurality of stages sequentially making an electrical contact with each other, each of the stages including a plurality of thin film transistors comprising amorphous silicon, and~~ including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register.